Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended and new claims added to clarify Applicants invention.

Support for the amended claims are found in the original claims and/or the Specification. No new matter has been added.

For example support for the amendments is found in the Specification at paragraphs 0035 and 0036:

[0035] Referring next to FIG. 3B, after the opaque layer 58 is deposited on the base dielectric layer 54, the substrate 52 is placed in a conventional focused ion beam chamber (not shown) and etched by a typically high current density of approximately 400-800 pA in the vicinity of the alignment marks 56. The FIB apparatus 62 typically uses a noble gas, typically argon, as an ion source 63. When used as the ion source 63, argon gas enhances the etch rate and selectivity of the focused ion beams 64 emitted from the FIB apparatus 62. Alternatively, the ion source 63 may be a liquid metal ion such as gallium. Accordingly, the FIB apparatus 62 is initially positioned over the portion of the metal layer 58 **which overlies the alignment marks 56. As the FIB process proceeds, the focused ion beams 64 uniformly etch away an opaque layer portion 60 corresponding to the entire thickness of the opaque layer 58, including possibly a thin slice of the**

underlying base dielectric layer 54. The progress of the material removal can be seen in a video monitor which indicates the layers that are removed in real time. The capability of the FIB apparatus 62 to **provide viewing of the opaque layer 58 and base dielectric layer 54 in real time** is of great benefit **which further facilitates proper cutting away of the opaque layer portion 60**. Furthermore, the current, voltage, size, ion flux and bombardment time of the focused ion beams 64 may be adjusted according to the knowledge of those skilled in the art to control the etching area of the focused ion beams 64. The bombardment area can be adjusted by tuning the ion beam size, the etching speed by tuning the ion flux, the etching depth by tuning the bombardment time, and the surface roughness by changing the ion energy and flux.

[0036] The focused ion beam cutting process continues **until the base dielectric layer 54 appears in the video monitor** of the FIB apparatus 62. At that point, the cutting process is terminated and an exposure opening 66 corresponding to the opaque layer portion 60 (FIG. 3B) removed from the opaque layer 58 **extends through the thickness of the layer 58**, as shown in FIG. 3C. **Due to the transparency of the base dielectric layer 54, the alignment marks 56 are again visible through the base dielectric layer 54, rendering it possible for personnel to properly align and position the substrate 52 in processing tools for subsequent semiconductor processing. Fabrication of the MIM capacitor on the substrate portion 50 is completed typically by depositing a second dielectric layer 68 on the opaque metal layer 58, after which a second metal layer 70 is typically deposited on the second dielectric layer 68.** At any point during the fabrication process, the second metal layer 70 or any other metal layer or layers sequentially deposited on the substrate 52 **to fabricate the MIM capacitor may be cut using the focused ion beams** 64, in the manner heretofore described with respect to FIG. 3B, in order to facilitate precise and time-efficient re-exposure of the alignment marks 56 on the substrate 52, as deemed necessary.

Claim Rejections under 35 USC 103

1. Claims 1, 2, 5, 9, 10, 13, 16, 17, and 19 stand rejected under 35 USC 103(a) as being unpatentable over Applicants alleged admitted prior art in view of Miller (US 2004/0099638).

In a discussion of the prior art and problems presented thereby, Applicants discuss at paragraphs 0011-0012:

A sectional view of a portion of a MIM capacitor 10 fabricated on a wafer substrate 12 is shown in FIG. 1. During fabrication of the MIM capacitor 10, a transparent base dielectric layer 14 is deposited on the substrate 12. Multiple alignment marks 16 are provided at the junction between the substrate 12 and the base dielectric layer 14 to facilitate proper alignment of the substrate 12 with various processing tool elements during semiconductor fabrication, as is known by those skilled in the art. **An opaque bottom metal layer 18 is deposited on the base dielectric layer 14, after which an intermetal dielectric layer 20 is deposited on the bottom metal layer 18. Finally, a top metal layer 22 is deposited on the intermetal dielectric layer 20. As shown, the alignment marks 16 are obscured by the overlying opaque bottom metal layer 18 and top metal layer 22.**

Conventional methods for re-exposing the alignment marks 16 after deposition of the metal layers 18, 22 on the substrate 12 include using standard photolithography techniques, in which a layer of photoresist 24 is initially patterned on the top metal layer 22. Next, photoresist stripping and etching techniques are used to remove aligned portions of the photoresist 24, the top metal layer 22, the intermetal dielectric layer 20 and the bottom metal layer 18, respectively, in order to expose the alignment marks 16 through the transparent base dielectric layer 14. However, this method is time-consuming, imprecise and produces supply bottlenecks under high-volume processing conditions. **Accordingly, a new and improved method for the expeditious,**

precise and time-efficient re-exposure of alignment marks during MIM capacitor fabrication is needed. According to the method of the present invention, this is achieved using focused ion beam (FIB) technology.

On the other hand Miller discloses using a focused ion beam (FIB) **to remove metallization layers covering alignment marks** (paragraph 0013, 0026), where the method includes **first calculating an ion beam dose** (paragraph 0046, 0047) at beam currents of 300 to 20,000 nanoamps (paragraph 0035) **necessary to uncover the alignment marks**. Miller discloses that adequate removal of the metallization layer may be confirmed by inspection with an optical microscope (paragraph 0047).

Any motivation to combine Miller with Applicants invention must necessarily impermissibly come from Applicants disclosure. For example nowhere does Miller disclose or suggest "A method of rendering visible alignment marks on a substrate through an overlying transparent dielectric layer on an upper surface of said substrate during semiconductor device fabrication"

Nevertheless, even assuming *arguendo* a proper motivation for combining the teachings of Miller (**metallization layer removal to uncover alignment marks** using an FIB with the teachings of Applicants who **teach etching through two metal**

layers and an IMD layer to expose alignment marks through a base dielectric (i.e., alignment marks are re-exposed by **photoresist stripping and etching techniques to remove aligned portions of the photoresist 24, the top metal layer 22, the intermetal dielectric layer 20 and the bottom metal layer 18, respectively, in order to expose the alignment marks 16 through the transparent base dielectric layer 14.)**, does not help Examiner in producing Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must **teach or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success **must both be found in the prior art, and not based on applicant's disclosure.**" *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

3. Claims 3, 11, and 18 stand rejected under 35 USC 103(a) as being unpatentable over Livengood et al., above in view of Lee et al. (US 6,251,782).

Applicants reiterate the comments made above with respect to Applicants alleged admitted prior art and Miller et al.

The fact that Lee et al. disclose a current density of 672 pA **to etch silicon** using an FIB system, which is outside the rang of the teachings of Miller (300 to 20,000 nanoamps) does not further help Examiner in producing Applicants disclosed and claimed invention or establishing a *prima facie* case of obviousness.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Conclusion

The cited references, either singly or in combination, do not produce Applicants disclosed and claimed invention and are therefore insufficient to make out a *prima facie* case of obviousness.

Applicants have amended their claims and new claims have been added to clarify Applicants disclosed and claimed invention.

Based on the foregoing, Applicants respectfully request reconsideration of the Claims and submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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